

CLAIMS

What is claimed is:

1. A method of determining the value of a memory element within a plurality of memory elements, comprising:
 - selecting a column of interest containing a desired memory element;
 - disabling the desired memory element;
 - measuring a first current provided to the column of interest;
 - adjusting measurement circuitry to compensate for skew introduced by undesired memory elements;
 - enabling the desired memory element; and
 - measuring a second current provided to the column of interest.
2. The method according to claim 1, wherein the memory elements comprise magnetic memory elements.
3. The method according to claim 2, wherein the memory elements further comprise magneto-resistive memory elements.
4. The method according to claim 1, wherein selecting a column of interest includes coupling voltages to various columns.
5. The method of claim 1, wherein disabling the desired memory element includes coupling the desired memory element to a high impedance state.
6. The method of claim 1, wherein disabling the desired memory element includes coupling the desired memory element to a known voltage.
7. The method of claim 1, wherein the current is measured using read circuitry coupled to the column of interest.
8. The method of claim 7, wherein adjusting includes altering the input offset voltage of the read circuitry.

9. The method of claim 7, wherein the first current measurement corresponds to the skew introduced by undesired memory elements.
10. The method of claim 7, wherein the second current measurement corresponds to the digital value of the desired memory element.
11. The method of claim 1, wherein enabling includes coupling the desired memory element to ground.
12. A method of evaluating magnetic memory, comprising:
 - selecting a column of interest containing a desired memory element;
 - measuring the current provided to the column of interest;
 - disabling the desired memory element;
 - enabling the desired memory element;
 - monitoring the measured current value during the disabling and enabling of the desired memory element.
13. The method of claim 12, wherein monitoring includes determining the derivative of the measured current value.
14. The method of claim 13, wherein the digital value of the memory element is indicated by the peak value of the derivative.
15. The method according to claim 14, wherein the memory elements comprise magnetic memory arrays.
16. The method according to claim 15, wherein the memory arrays further comprise magneto-resistive memory elements.
17. A memory, comprising:
 - a plurality of memory elements;

a gain stage coupled to the plurality of memory elements; and
a controller coupled to the plurality of memory elements and the gain stage;
wherein the controller is capable of providing a current to the plurality of memory elements;
wherein the gain stage may establish a voltage at the plurality of memory elements by modulating the amount of current provided by the controller.

18. The memory of claim 17, wherein the plurality of memory elements include a desired memory element and undesired memory elements.

19. The memory of claim 18, further comprising a switch for coupling the desired memory element to a plurality of known states.

20. The memory of claim 19, wherein the known state is a high impedance state.

21. The memory of claim 20, wherein the current provided by the controller is measured to determine the amount of skew contributed by the undesired memory elements.

22. The memory of claim 21, wherein the gain stage is compensated to account for the skew caused by the undesired memory elements.

23. The memory of claim 19, wherein the known state is ground.

24. The memory of claim 19, wherein the gain stage has been compensated to account for skew caused by the undesired memory elements.

25. The memory of claim 24, wherein the current provided by the controller corresponds to the digital value of the memory element.

26. The memory of claim 24, wherein compensating the gain stage includes adjusting its input offset voltage.
27. The memory of claim 19, wherein the switch comprises a tri-state buffer.
28. The memory of claim 18, wherein the plurality of memory elements further comprise magnetic memory elements.
29. The memory of claim 28, wherein the plurality of memory elements further comprise magneto-resistive memory elements.
30. The memory of claim 19, wherein the plurality of known states include a state where the desired memory element is enabled and a state where the desired memory element is disabled.
31. The memory of claim 30, wherein the difference in the magnitude of current provided by the controller with the desired memory element in the enabled and disabled states correlates to the digital value of the desired memory element.
32. A computer system, comprising:
a central processing unit ("CPU");
a memory device coupled to the CPU, wherein the memory comprises:
a plurality of memory elements;
a gain stage coupled to the plurality of memory elements; and
a controller coupled to the plurality of memory elements and the gain stage wherein the controller is capable of providing a current to the plurality of memory elements;
wherein the gain stage may establish a voltage at the plurality of memory elements by modulating the amount of current provided by the controller.

33. The computer of claim 32, wherein the plurality of memory elements include a desired memory element and undesired memory elements.

34. The computer of claim 33, wherein the memory further comprises a switch for coupling the desired memory element to a plurality of known states.

35. The computer of claim 33, wherein the plurality of known states include a state where the desired memory element is enabled and a state where the desired memory element is disabled.

36. A memory, comprising:
a plurality of memory elements including a desired memory element and undesired memory elements;
means for providing a current to the plurality of memory elements; and
establishing a voltage at the plurality of memory elements.

37. The memory of claim 36, further comprising a means for coupling the desired memory element to a known state.

38. The memory of claim 36, further comprising a means for isolating the desired memory element from the undesired memory elements.

39. The memory of claim 38, further comprising a means for determining the digital value of the desired memory.